REMARKS

The following remarks are provided in response to the Office Action mailed August 3, 2005 in which the Examiner:

- rejected claims 1-5 under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 5,972,123 to Verhaverbeke or United States Patent No. 6,015,505 to David et al.
- rejected claims 6-20 under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 5,972,123 to Verhaverbeke (hereinafter Verhaverbeke) in view of United States Patent No. 6,902,969 to Adetutu et al. (herein after Adetutu) or US 2004/0191974 to Gilmer et al. (hereinafter Gilmer).

Claims 1-5 are herein cancelled. The applicants respectfully request reconsideration of the above referenced patent application in view of the remarks set forth herein, and respectfully request that the Examiner withdraw all rejections.

New Claims

The applicants herein add new claims 21-30 and submit that they have the right to claim the invention as set forth in the new claims.

35 U.S.C. §103(a)

The Examiner rejected claims 6-20 under §103(a) as being unpatentable over Verhaverbeke in view of Adetutu or Gilmer. For at least the following reasons the applicants traverse the Examiner's rejection.

A *prima facie* case of obviousness under 35 U.S.C. §103 requires three criteria:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest **all** the claim limitations (emphasis added).
> M.P.E.P. §2143

To overcome a §103(a) rejection, the applicants must only demonstrate that the Examiner has failed to establish one of the criteria required for a *prima facie* case of obviousness.

The applicants will respond to the Examiner's §103 rejection with respect to amended independent claims 6, 11 and 16. In these claims, the applicants teach and claim a method of forming one or more metal layers on a substrate or a high-k gate dielectric layer, said one or more metal layers having a thickness, forming a masking layer on said metal layer, exposing part of said one or more metal layers, and applying a wet etchant that comprises an active ingredient (e.g. a chelating agent) to remove said exposed part of said one ore more metal layers from said substrate or said high-k gate dielectric layer, wherein, **the diameter of said active ingredient exceeds the total thickness of said one or more metal layers**. By ensuring that the active ingredient in the wet etchant is larger than the thickness of the material being etched, the undercut of the metal layer under a masking layer is mitigated, inhibiting a significant isotropic undercut etch. The resulting profile of the etched metal layer in inherently anisotropic.

Verhaverbeke fails to disclose or render obvious a method of wet etching the exposed portion of a metal layer wherein the physical dimensions of the active component of the wet etchant (e.g. a chelating agent) encumbers the undercutting of said

metal layer underneath a masking layer, effectively mitigating a significant loss of said metal layer from underneath said masking layer. Verhaverbeke discloses a method of "cleaning or etching semiconductor wafers, and particularly . . . oxide etching semiconductor wafers, using a cleaning etching aqueous solution that contains ammonium fluoride (NH_4F) and preferably also contains hydrogen fluoride (HF)" (Figs. **1-4**) (col. 2, lines 20-26). The advantages disclosed by Verhaverbeke include easy incorporation into the semiconductor processor manufacturing process "without significant retrofitting because the raw material reagents . . . are already used for other processing steps" (col. 2, lines 36-41), reduction of particle issues in the processing system (Fig. **5**) (col. 2, lines 44-46), improved etch uniformity over conventional buffered hydrogen fluoride techniques (col. 2, lines 46-48), improved purity for the buffered hydrogen fluoride solution with a lower concentration of metallic impurities (col. 2, lines 47-50), and the enabling of "any mixing ratio at point of use providing increased processing flexibility" (col. 2, lines 50-52). Verhaverbeke does not disclose a relationship between the size of the active etchant and the proportions of the material being etched. Therefore, Verhaverbeke does not disclose the method of mitigating the undercut of a metal layer underneath a masking layer by ensuring that the diameter of the active etchant exceeds that of said metal film being etched.

Adetutu also does not teach a method of wet etching wherein the diameter of an active species in a wet etchant is larger than the thickness of a metal film being etched in order to inhibit a significant amount of undercut of the metal film under a masking layer. Adetutu discloses a method "that enables the manufacturing of an integrated circuit

employing a first type of gate electrode for a first type of devices and a second type of gate electrode for a second type of devices" (col. 2, lines 1-3). Adetutu addresses problems typically associated with dual gates structures **137** and **139**, namely, poor selectivity during the gate electrode etch process resulting in undesired etching and/or gouging of the gate dielectric **114** and/or semiconductor substrate **112**, by incorporating an etch stop layer **115** that is highly selective to the dual gate etch species (col. 2, lines 4-8). The presence of the etch stop layer **115** prevents the gate stack etch process from undesirably etching the underlying gate dielectric **114** and wafer substrate **112** (col. 2, lines 10-14). Therefore, Adetutu does not disclose the method of specifying the diameter of the etchant that etches a metal layer, as taught by the applicants.

Gilmer as well fails to disclose or render obvious a method of wet etching the exposed portion of a metal layer such that the size of the active etchant exceeds the thickness of the metal layer being etched, thereby hampering the undercutting of said metal layer underneath a masking layer. Gilmer describes a method of "fabricating a semiconductor device, such as, for example, a CMOS transistor, having an integrated gate conductor that is formed from at least two, respectively different, metallic materials" [0018], wherein such a process "introduces the opportunity to cause damage to the gate dielectric material [**34**]" [0026]. By interposing a sacrificial layer over the gate dielectric material **34** in anticipation of the metal removal step [0026], Gilmer discloses a remedy wherein "the gate dielectric easily withstands the wet chemical etch . . . used to remove the sacrificial layer" [0026]. Therefore, Gilmer does not disclose the method of mitigating the undercut of a metal layer underneath a masking layer by ensuring that the

diameter of the active etchant exceeds that of said metal film being etched.

Since none of Verhaverbeke, Adetutu nor Gilmer disclose the method taught by the applicants, the applicants respectfully request the removal of the U.S.C. §103(a) rejection of independent claims 6, 11 and 16. Additionally, new independent claims 21 and 25 should be considered in light of the arguments presented above. The applicants further submit that amended dependent claims 7-10, 12-15 and 17-20 and new dependent claims 22-24 and 26-30 are patentable as each depends from a nonobvious independent claim. (See M.P.E.P. §2143.03 (citing In re Fine, 5 U.S.P.Q.2d (BNA) 1596 (Fed. Cir. 1988))).

CONCLUSION

For at least the foregoing reasons, the applicants submit that they have overcome the Examiner's rejection and that they have the right to claim the invention as set forth in the listed claims. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, L.L.P.

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Dated

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